VPlan + RV: A Proposal

Simon Moll and Sebastian Hack

October 18, 2017

http://compilers.cs.uni-saarland.de

Compiler Design Lab
Saarland University

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  for (int k=n; k>=0; k--) {
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$\rightarrow$ The Region Vectorizer can.

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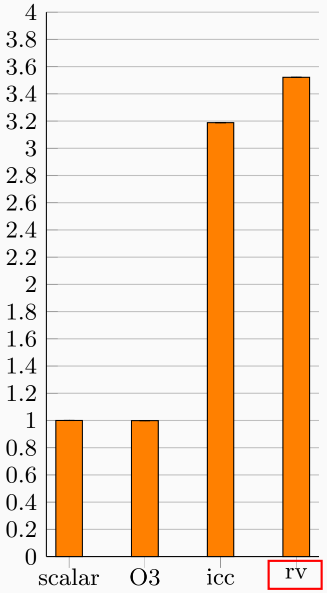
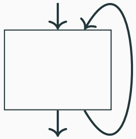


LLVM's LoopVectorizer

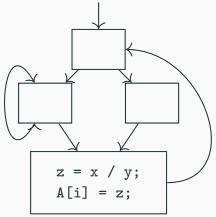


- only loops.
- only inner loops.
- only a single basic block (will if-convert all control flow).
- only very basic reduction patterns.
- complex, interdependent code base.

VPlan: Future of Vectorization in LLVM.

VPlan

Tentative plan to vectorize an (outer) loop without changing the IR.



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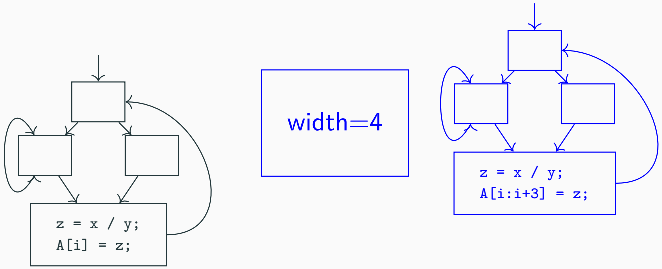

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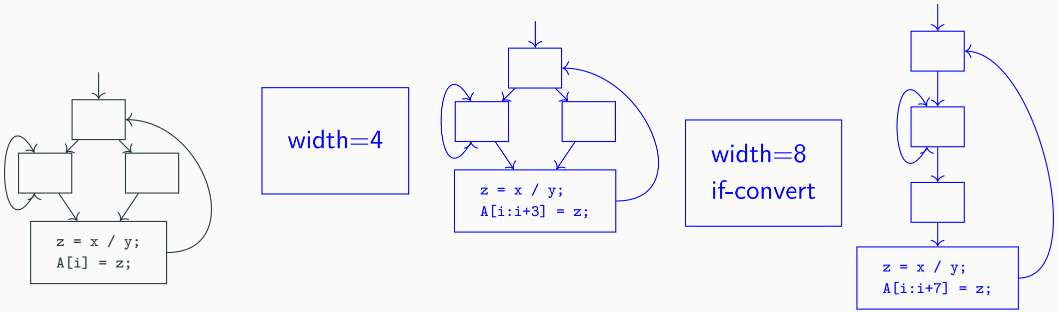

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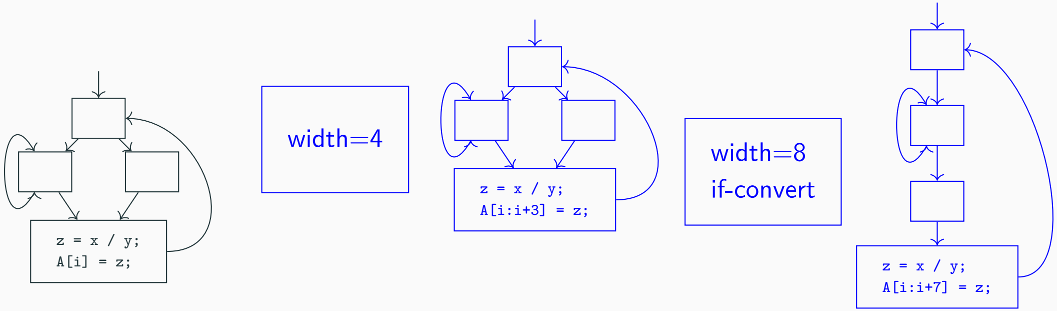

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Already available in RV.

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RV: The Region Vectorizer

Whole-Function **and** Outer-Loop Vectorizer.

- **powerful** strong analyses & transformations.
- **robust** vectorize any control-flow.
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Aren't those two separate paradigms?

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Wrap body in loop and Loop Vectorize. [VecClone Pass, D22792]

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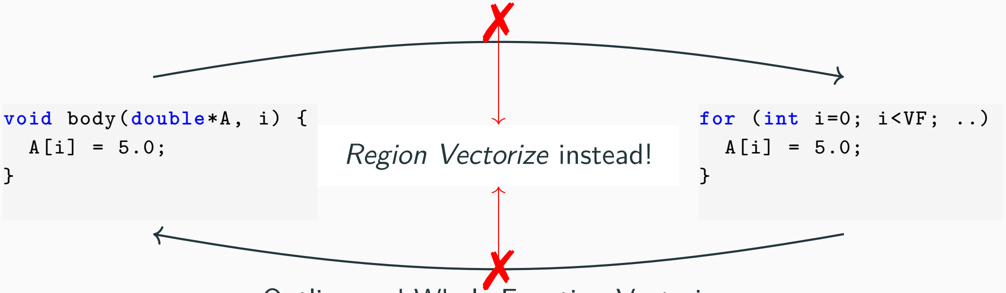

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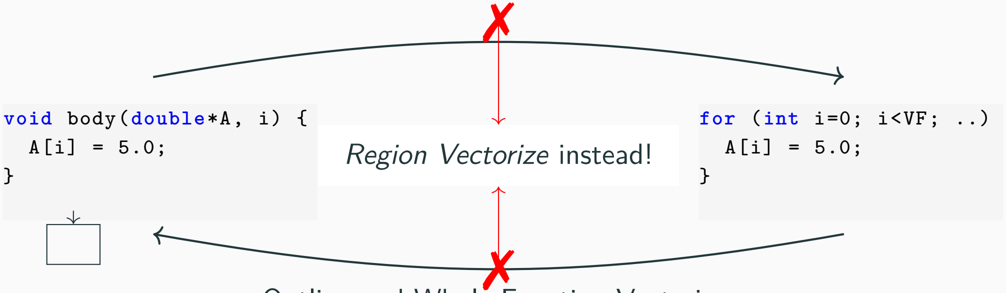

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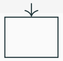

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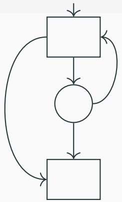

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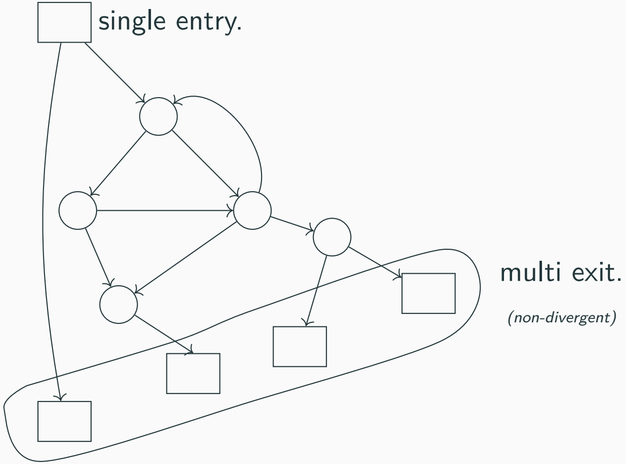

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for (int i = 0; i<n; ++i) {
  ...
  continue;
  ...
}
```

```
double func(..) {
  ..  return 42.0; ..
  ..  return v;
}
```

rv::Region

To RV, loop vectorization and whole-function vectorization are (almost) the same.

RV architecture

Divergence Analysis

Recurrence Analysis

Alloca Opt.

BOSCC Heuristics

Partial Linearization

Vector IR Generator

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- SLEEF vector math (AVX2, AVX512, Advanced SIMD, ..)

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- **No questions asked.** Incomplete legality checks
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→ these missing parts are already in VPlan/LLVM

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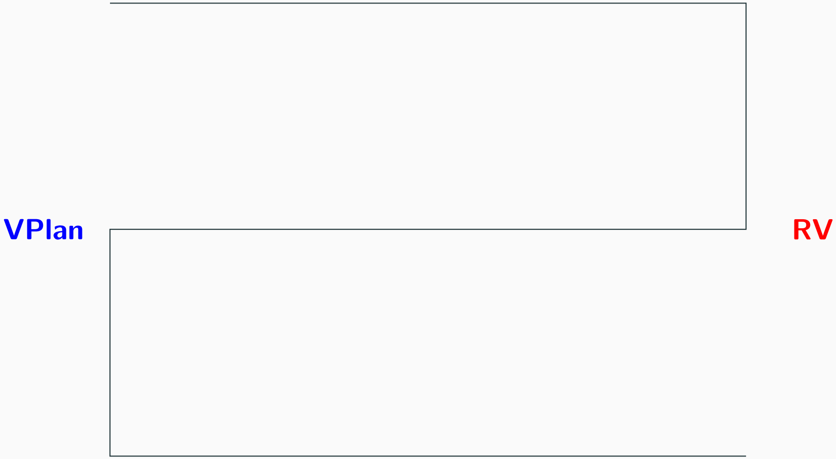

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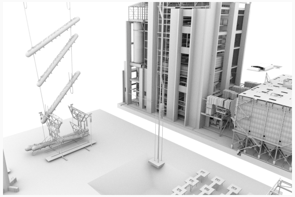
Divergence Analysis Stress Test: Rodent



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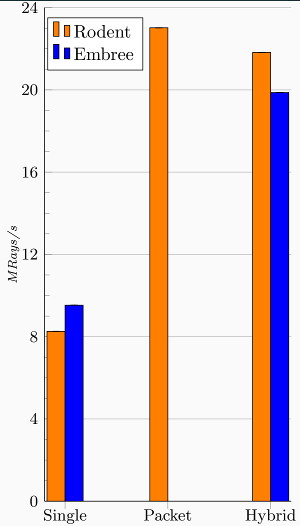

Clang 4.0, AO rays, BVH8, AVX2, i7 6700K

Joint Effort with Intel

Let's upstream RV's divergence analysis!

- Joint Effort with Intel to integrate *Divergence Analysis* of RV into VPlan.
- Design Goals
  - no regressions compared to current SCEV-based implementation.
  - precise sync dependences.

Conclusion

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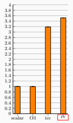

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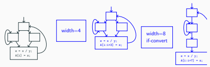

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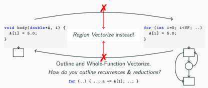

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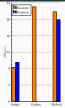

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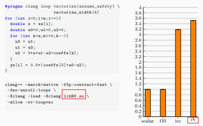

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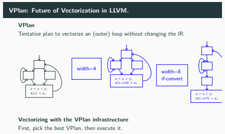

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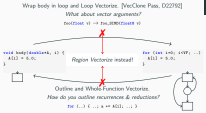
VPlan

Tentative plan to vectorize an (outer) loop without changing the IR.

Vectorizing with the VPlan infrastructure

First, pick the best VPlan, then execute it.



Wrap body in loop and Loop Vectorize. [VecClone Pass, D22792]

What about vector arguments?

`foo(float v) → foo_SIMD(float8 v)`

```
void body(double*A, i) {
  A[i] = 5.0;
}
```

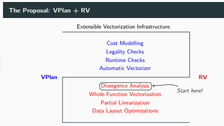
Region Vectorize instead!

```
for (int i=0; i<VF; ..)
  A[i] = 5.0;
}
```

Outline and Whole-Function Vectorize.

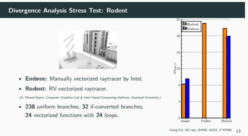
How do you outline recurrences & reductions?

`for (..) { ..; a += A[i]; ..; }`



The Proposal: VPlan + RV

Extensible Vectorization Infrastructure.



Divergence Analysis Stress Test: Rodent

- **Embree:** Manually vectorized raytracer by Intel.
- **Rodent:** RV-vectorized raytracer.

(A. Pérard-Gayot, Computer Graphics Lab & Intel Visual Computing Institute, Saarland University)

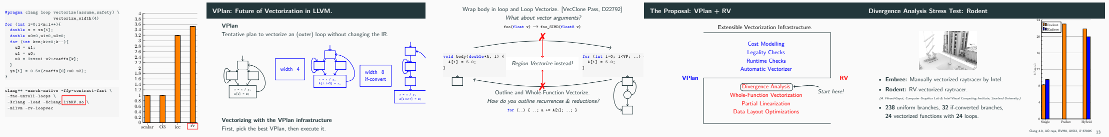
- **238** uniform branches, **32** if-converted branches, **24** vectorized functions with **24** loops.

Clang 4.0, AO rays, BVH8, AVX2, i7 6700K 13

RV Team

Thorsten Klössner Dominik Montada Arsène Pérard-Gayot Simon Moll

Conclusion


VPlan: Future of Vectorization in LLVM.
Wrap body in loop and Loop Vectorize. [VecClone Pass, D22792]
Region Vectorize instead!
Outline and Whole-Function Vectorize.
The Proposal: VPlan + RV
Extensible Vectorization Infrastructure.
Divergence Analysis Stress Test: Rodent

RV Team

Thorsten Klössner   Dominik Montada   Arsène Pérard-Gayot   Simon Moll

VPlan talk, today 4:20pm

Vectorizing Loops with VPlan – Current State and Next Steps, Ayal Zaks

Backup

RV: A Unified Region Vectorizer for LLVM

Simon Moll / Saarland University / Saarland Informatics Campus

SAARLAND UNIVERSITY
COMPUTER SCIENCE

Introduction

The Region Vectorizer provides a single, unified API to vectorize code regions.

- RV is a generalization of the Whole-Function Vectorizer
  R. Karrenberg, S. Hack, "Whole Function Vectorization" (CGO '11)

```
rv::VectorizationInfo vi;
// region set up
rv::Region R(xLoop);
vi.setVectorShape(xPhi,
        VectorShape::consecutive());

// Vectorization analysis
rv::analyze(R, vi, domTree, loopInfo);

// Control conversion
rv::linearize(R, vi, domTree, loopInfo);

// Vector IR generation
rv::vectorize(R, vi, domTree);
```

Applications

- **Outer-Loop Vectorizer** An "unroll-and-jam" vectorizer based on RV's analysis and transformations
- **`pragma omp simd`** Emit vector code for SIMD regions right from Clang
- **Vectorizer Cost Model** How much predication? Which memory accesses vectorize well?
- **Polly** Directly vectorize loops during Polly code generation
- **PIR** Parallel region vectorizer

`rv::Region` Region

A region can be a subset of the basic blocks in a function or an entire function (`omp declare simd`).

```
#pragma omp simd
for (int x = 0; x < width; ++x) {
  for (int y = 0; y < height; ++y) {
    complex<double> c = (startX+x*step) + (startY-y*step) * I;
    complex<double> z = 0.0;

    for (int n = 0; n < MAX_ITER; ++n) {
      z = z * z + c;
      if (hypot(z.real, z.imag) >= ESCAPE)
        break;
    }                                              divergent loop
    buffer[y][x] = colorMap(z);
  }
}
```

```
#pragma omp declare simd
float min (float a, float b)
{
    if (a < b) return a; else return b;
}
```

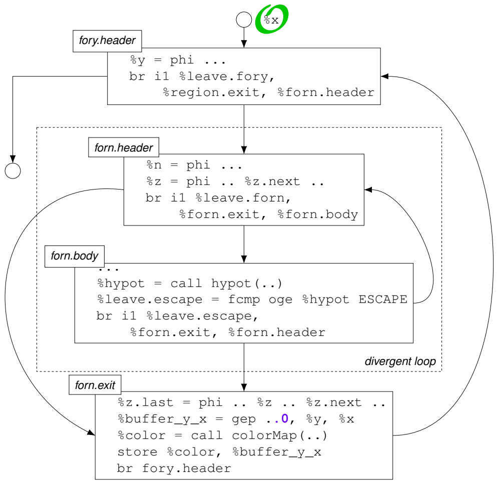
↓

```
float min_v8 (<8 x float> a, <8 x float> b) {
  return select(a < b, a, b);
}
```

```
        break;
  }                                                divergent loop
  buffer[y][x] = colorMap(z);
 }
}
```

```
    return select(a < b, a, b);
}
```

rv::analyze   Vectorization Analysis



```
fory.header:
  %y = phi ...
  br i1 %leave.fory,
       %region.exit, %forn.header

forn.header:
  %n = phi ...
  %z = phi .. %z.next ..
  br i1 %leave.forn,
       %forn.exit, %forn.body

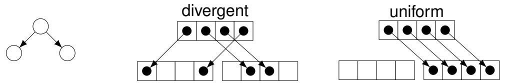
forn.body:
  ...
  %hypot = call hypot(..)
  %leave.escape = fcmp oge %hypot ESCAPE
  br i1 %leave.escape,
       %forn.exit, %forn.header

forn.exit:
  %z.last = phi .. %z .. %z.next ..
  %buffer_y_x = gep ..0, %y, %x
  %color = call colorMap(..)
  store %color, %buffer_y_x
  br fory.header
```

					(*stride*, *alignment*) or ⊤	
i64	%x	0 1 2 3	4 5 6 7	...	**(1, 4)**	*(consecutive)*
i64	%y, %n	3 3 3 3	4 4 4 4	...	**(0, 1)**	*(uniform)*
i1	%leave.escape	1 1 0 0	0 0 1 1	...	⊤	*(varying)*

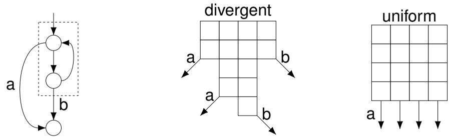
Branch Divergence

Which branches cause SIMD threads to diverge?



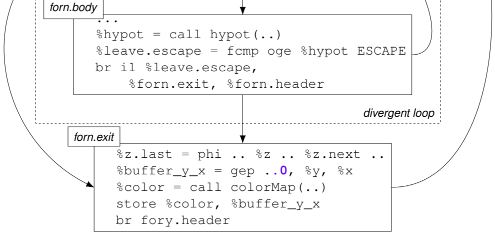
Loop Divergence

Which loops drop off SIMD threads at different exits?



rv::linearize   Control Conversion

- Optimized linearization of divergent branches

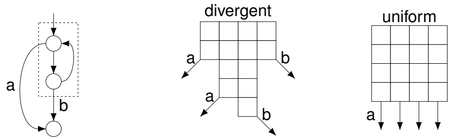


```
...
%hypot = call hypot(..)
%leave.escape = fcmp oge %hypot ESCAPE
br i1 %leave.escape,
    %forn.exit, %forn.header
```

```
%z.last = phi .. %z .. %z.next ..
%buffer_y_x = gep ..0, %y, %x
%color = call colorMap(..)
store %color, %buffer_y_x
br fory.header
```

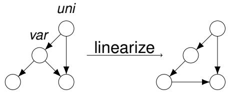
Loop Divergence

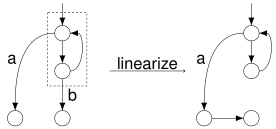
Which loops drop off SIMD threads at different exits?



`rv::linearize` Control Conversion

- Optimized linearization of divergent branches and loops (→ predication)
- Preserves uniform branches and loops
- Generates Predicated IR
  1. All branches are uniform
  2. Blocks may be predicated





Future Work

- BOSCC (skip predicated regions if no SIMD thread is active)
  J. Shin, "Introducing Control Flow into Vectorized Code" (PACT '07)
- Multi-dimensional Analysis
  C. Yount, "Vector Folding: Improving Stencil Performance via Multi-dimensional SIMD-vector Representation" (ICESS-CSS-HPCC '15)
- Vectorization of interleaved memory accesses
- Integration with Clang / LoopVectorizer / Polly
- Reductions

  - Development available at GitHub
    `https://github.com/simoll/rv`

moll@cs.uni-saarland.de